PATENT ABSTRACTS OF JAPAN

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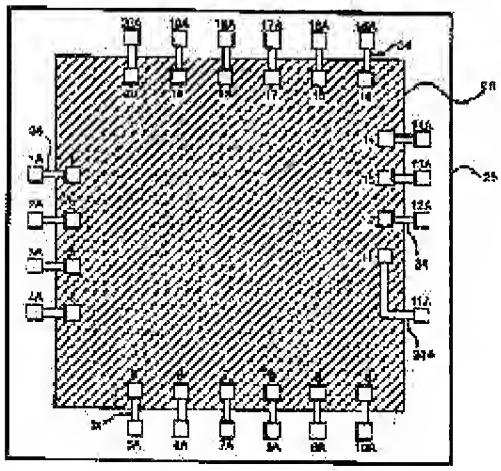
(54) SEMICONDUCTOR DEVICE



(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device executing wire bonding without damaging elements on a semiconductor chip.
SOLUTION: At least pads for bump and pads for wire bonding are provided for one input/output terminal in pad structure on a semiconductor chip. The pads for bump 1-20 are installed in an area 26 where elements on the semiconductor chip 25 exist and the pads for wire bonding 1A-20A are installed out of the area 26. Then, the pads are mutually connected.

CLAIMS

[Claim(s)]
[Claim 1]In what is provided with both a pad for vamps, and a pad for wirebonding at least to one input/output terminal about pad structure on a semiconductor chip, Said pad for wirebonding is that to which wirebonding is performed via an opening of a chip protective film formed on wiring for wirebonding, A semiconductor device having provided said pad for wirebonding outside said field, and connecting these pads of each

other while providing said pad for vamps in a field where an element on a semiconductor chip exists.
[Claim 2]In what is provided with both a pad for vamps, and a pad for wirebonding at least to one input/output terminal about pad structure on a semiconductor chip which consists of quadrilaterals, Wirebonding is performed via an opening of a chip protective film formed on wiring for wirebonding, and said pad for wirebonding corresponds each neighborhood of a semiconductor chip which consists of quadrilaterals, While providing two or more pads for vamps in a field where an element on a semiconductor chip exists, respectively and allocating all the pads for vamps of these each neighborhood in center-section slippage of each neighborhood rather than a pad for vamps of an adjoining neighborhood, The semiconductor device according to claim 1 connecting these pads of each other that counter said pad for vamps, allocate two or more pads for wirebonding along with semiconductor chip each neighborhood, respectively, and belong to the same input/output terminal.
[Claim 3]The semiconductor device according to claim 1 or 2 which aperture shape of a pad for vamps is circular, and aperture shape of a pad for wirebonding is a rectangle, and is characterized by both aperture shape differing.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001] [Field of the Invention]This invention is a semiconductor device and a thing concerning the pad structure of a semiconductor chip especially.
[0002] [Description of the Prior Art]Drawing 3 is an example which shows the conventional semiconductor chip. In a figure, 1 to 20 is the pad region for vamps formed on the semiconductor chip 25. 26 shows the field where the element on the semiconductor chip 25 exists.
[0003]Drawing 4 is an enlarged drawing of the pad region for vamps shown in drawing 3. In a figure, 33 shows the opening of the chip protective film formed on the aluminum wiring 32.
[0004]Drawing 5 is the sectional view of a vamp formed on the pad region for vamps shown in drawing 4. In a figure, 35 is the vamp ball connected to the aluminum wiring 37 formed on the silicon substrate 40 via the ground metal 38. 36 is a chip protective film and 39 is an interlayer film.
[0005]Next, the morphosis of each part in the manufacturing process of the conventional semiconductor device is explained. First, the pad regions 1-20 for vamps are formed on the semiconductor chip 25 as shown in drawing 3. The shape of the pad region for vamps is as being shown in drawing 4.
The opening 33 of a chip protective film is [that it is the optimal shape for bump shape, and] circular.

[0006]Thus, on the formed pad region for vamps, the vamp ball 35 is connected via the ground metal 38 for improving adhesion with the aluminum wiring 37 as shown in drawing 5. Although many techniques are enforced about formation of the concrete vamp, since it is unrelated to the essence of this invention, explanation is omitted.

[0007] [Problem(s) to be Solved by the Invention]Since the conventional semiconductor device is constituted as mentioned above, there is a problem as shown below. A valuation method does not exist besides usually mounting the semiconductor chip in which the vamp was formed in a substrate. By the time it evaluates, creation of an exclusive base, formation of a vamp, and also mounting to a substrate are required, and it has become the hindrance for carrying out quick evaluation. Therefore, for quick evaluation, the needs to carry out the same packaging as usual are strong without forming a vamp, even if it is a semiconductor chip for forming a vamp.
[0008]However, since a damage occurs to an element when the pad regions 1-20 for vamps are formed in the field 26 which exists in the element on the semiconductor chip 25 as shown in drawing 3, it is impossible to carry out a wire bond. This problem is avoidable by arranging the pad region for vamps outside the field 26 where the element on the semiconductor chip 25 exists.
[0009]However, since the opening 33 of a chip protective film is circular as shown in drawing 4, it is not suitable for a wire bond. Anyway, the problem that it is impossible and packaging cannot be carried out generates a wire bond.
[0010]Even if it is a case where packaging does not have to be carried out at all, the problem in connection with a wafer test exists. That is, like the above, when doing the wafer test by general needle contact, since the opening 33 of a chip protective film is circular, securing the margin of the contact place of a needle needs a difficult and higher-precision device.
[0011]When a wafer test is carried out, the crack by the needle having contacted on the aluminum wiring 32 shown in drawing 4 is made. In many cases, two or more cracks occur, and trouble is caused when forming a vamp. Although what is necessary is just to test after forming a vamp in order to avoid this, a device for exclusive use is needed too. Anyway, since the conventional wafer test device cannot use it as it is, problems, like new plant-and-equipment investment is needed occur.
[0012]This invention is made in order to cancel the above problems, and if a damage is given to the element on a semiconductor chip, it will make the semiconductor device of composition of that wire-bond-work ** can be performed appropriately that there is nothing profitably like.
[0013]As conventional technology by a publication, although there are JP,8-29451,A, JP,5-129305,A, and JP,7-201866,A, there is no statement in these per solving means of the technical problem mentioned above, and these inventions differ in technical thought.
[0014] [Means for Solving the Problem]In what is provided with both a pad for vamps, and a pad for wirebonding at least to one input/output terminal about pad structure on a semiconductor chip in a semiconductor device concerning the 1st invention, Said pad for wirebonding is that to which wirebonding is performed via an opening of a chip protective film formed on wiring for wirebonding, While providing said pad for vamps in a field where an element on a semiconductor chip exists, said pad for wirebonding is provided outside said field, and these pads of each other are connected.
[0015]In a semiconductor device concerning the 2nd invention, one input/output terminal is received in the 1st invention about pad structure on a semiconductor chip which consists of quadrilaterals, In what is provided with both a pad for vamps, and a pad for wirebonding at least, Wirebonding is performed via an opening of a chip protective film formed on wiring for wirebonding, and said pad for wirebonding corresponds each

neighborhood of a semiconductor chip which consists of quadrilaterals, While providing two or more pads for vamps in a field where an element on a semiconductor chip exists, respectively and allocating all the pads for vamps of these each neighborhood in center-section slippage of each neighborhood rather than a pad for vamps of an adjoining neighborhood, Respectively said pad for vamps is countered, two or more pads for wirebonding are allocated along with semiconductor chip each neighborhood, and these pads of each other belonging to the same input/output terminal are connected.

[0016]Aperture shape of a pad for vamps is circular, and aperture shape of a pad for wirebonding is a rectangle, and it is made for both aperture shape to differ in the 1st or 2nd invention in a semiconductor device concerning the 3rd invention.

[0017] [Embodiment of the Invention]Embodiment 1. drawing 1 is a top view showing the embodiment of the semiconductor device of this invention. In a figure, 1 to 20 is the pad region for vamps formed on the semiconductor chip 25. 1A to 20A is a pad region for wirebonding, or a pad region for wafer tests. 26 shows the field where the element on the semiconductor chip 25 exists.

[0018]Drawing 2 is an enlarged drawing of the pad region for vamps shown in drawing 1 and the pad region for wirebonding, or the pad region for wafer tests. In a figure, 33 shows the opening of the chip protective film formed on the aluminum wiring 32 for vamps. 31 shows the opening of the chip protective film formed on the object for wirebonding, or the aluminum wiring 30 for wafer tests. Interconnection of the aluminum wiring 32 for vamps and the object for wirebonding, or the aluminum wiring 30 for wafer tests is carried out with the aluminum wiring 34 for pad connection. In 20A, from the pad region for wirebonding, or the pad region 1A for wafer tests, each field, It is constituted so that wirebonding work or wafer test work can be done via the opening 31 of the chip protective film formed on the object for wirebonding, or the aluminum wiring 30 for wafer tests, respectively.

[0019]Next, the morphosis of each part in the manufacturing process of a semiconductor device is explained. First, the pad regions 1-20 for vamps are formed on the semiconductor chip 25. 1A to 20A which is a pad region for wirebonding or a pad region for wafer tests is formed similarly to it. Although said pad regions 1-20 for vamps are formed in the field 26 where the element on the semiconductor chip 25 exists in that case, 1A to 20A which is said pad region for wirebonding or a pad region for wafer tests avoids the field 26 where said element exists, and is formed.

[0020]Said pad regions 1-20 for vamps are allocated corresponding to each neighborhood of the semiconductor chip 25 which makes a quadrilateral. Namely, the pad regions 1-4 for vamps are allocated in line on a straight line in the form corresponding to the graphic display left side of the semiconductor chip 25, and the pad regions 5-10 for vamps, It is allocated in line on a straight line in the form corresponding to the graphic display lower side of the semiconductor chip 25, and the pad regions 11-14 for vamps, It is allocated in line on a straight line in the form corresponding to the graphic display right-hand side of the semiconductor chip 25, and the pad regions 15-20 for vamps are allocated in line on the straight line in the form corresponding to the graphic display right-hand side of the semiconductor chip 25.

[0021]And all the pad regions of the pad regions 1-4 for vamps allocated corresponding to the left side of the semiconductor chip 25, It is allocated in center-section slippage of the left side of the semiconductor chip 25 rather than the pad regions 5-10 for vamps and

the pad regions 15-20 for vamps which were allocated corresponding to the lower side and the top chord which adjoin the left side of the semiconductor chip 25. Namely, all the pad regions 1-4 for vamps. In drawing 1, it is caudad allocated rather than the pad regions 15-20 for vamps which were allocated up in drawing 1 rather than the pad regions 5-10 for vamps allocated corresponding to the lower side of the semiconductor chip 25, and were allocated corresponding to the top chord of the semiconductor chip 25.
[0022]In each neighborhood similarly the pads 5-10 for vamps allocated corresponding to the lower side of the semiconductor chip 25, the pads 11-14 for vamps allocated corresponding to the right-hand side of the semiconductor chip 25, and the pads 15-20 for vamps allocated corresponding to the top chord of the semiconductor chip 25, It is allocated in center-section slippage of the neighborhood rather than the pad for vamps of the neighborhood which adjoins in all the pads for vamps.
[0023]And each of 20A counters each of the pad regions 1-20 for vamps from the pad region for wirebonding, or the pad region 1A for wafer tests, and it is allocated along with each neighborhood of the semiconductor chip 25. That is, each of 4A counters each of the pad regions 1-4 for vamps from the pad region for wirebonding, or the pad region 1A for wafer tests, and it is arranged on the straight line along the lower side shown in drawing 1 of the semiconductor chip 25.
[0024]Similarly From the pad region for wirebonding, or the pad region 5A for wafer tests to 10A. From the pad region for wirebonding, or the pad region 11A for wafer tests to 14A. And each of the pad region for wirebonding or the pad region 1A for wafer tests to 4A, Each of the pad regions 5-10 for vamps, the pad regions 11-14 for vamps, and the pad regions 15-20 for vamps is countered, and it is arranged on the straight line along with the lower side, the right-hand side, and the top chord which are shown in drawing 1 of the semiconductor chip 25.
[0025]The pad region 1 for vamps, the pad for wirebonding or the pad regions 1A and 2 for wafer tests which counter mutually and belong to the same input/output terminal, 2A, 3, 3A and ....., and 20 and 20A, It intersects perpendicularly with the boundary of the field 26 where the element on the semiconductor chip 25 exists with the aluminum wiring 34 for pad connection shown in drawing 2, respectively except for 11 and 11A, interconnection is carried out linearly, and it has a brief connection structure. The pad region 11 for vamps, the pad for wirebonding, or the pad region 11A for wafer tests, Interconnection is carried out with the aluminum wiring 34a for pad connection which consists of a portion which intersects perpendicularly with the boundary of the field 26 where the element on the semiconductor chip 25 exists, and extends linearly, and a portion which extends in parallel with the neighborhood of the semiconductor chip 25.
[0026]The shape of each pad region is as being shown in drawing 2, and the opening 33 of the chip protective film on the aluminum wiring 32 for vamps is [that it is the optimal shape for bump formation, and] circular. The opening 31 of the object for wirebonding or the chip protective film on the aluminum wiring 30 for wafer tests is wirebonding or the optimal shape for a wafer test. The object for wirebonding which had the opening 31 of the aluminum wiring 32 for vamps which had the opening 33 of a chip protective film formed, and a chip protective film formed, or the aluminum wiring 30 for wafer tests, Interconnection is carried out by connection structure brief as a whole with said aluminum wiring 34 and 34a for pad connection.
[0027]Originally, although the semiconductor chip 25 aims at vamp mounting, its needs

of packaging are strong as aforementioned. In that case, packaging can be easily carried out with the completely same technique as usual by carrying out a wire bond to 20A from 1A which is a pad region for wirebonding. That is, under 1A to 20A which is a pad region for wirebonding, since an element does not exist, there is no influence of the damage to an element, and the opening 31 of the chip protective film serves as the optimal shape for wirebonding.

[0028]Thus, in [according to the embodiment by this invention] 20A from the pad region 1A for wirebonding, Each pad region for wirebonding can do wirebonding work appropriately via the opening 31 of the chip protective film formed on the aluminum wiring 30 for wirebonding, and can respond also to packaging exactly. The greatest feature in this invention is being able to respond to both vamp mounting and packaging with the same chip, and the prominent effect that quick evaluation is attained is acquired. On the other hand, in the thing of JP,8-29451,A previously quoted as conventional technology, although there is a description a "bond pad", wirebonding is not performed and "the pads for wirebonding" said to this invention differs clearly. And in the thing of this Prior art, although the opening for vamps and the opening for wafer tests are formed eventually, the opening for wirebonding is not formed. in the case of this Prior art, it is impossible to actually carry out wirebonding for such a constitutional reason, and there is no statement concerning the pad for wirebonding also in contents. It is clear that it is different from this invention.

[0029]In the embodiment by this invention, when doing a wafer test, a wafer test can be done with the completely same technique as usual by carrying out per needle of 1A to 20A which is a pad region for wafer tests. That is, the opening 31 of the chip protective film serves as the optimal shape for a wafer test, and also even if two or more cracks attach a wafer test on the aluminum wiring 30 for wafer tests by carrying out multiple-times operation, it does not affect formation of a vamp at all.

[0030]And as mentioned above 20A from the pad for wirebonding, or the pad region 1A for wafer tests, Since it is allocated in line by center-section slippage of each neighborhood of the semiconductor chip 25 on the straight line along with each neighborhood, in using as a pad for wirebonding, When wirebonding work can be done appropriately, without being influenced by existence of the pad of other neighborhoods and it uses as a pad for wafer tests, wafer test work can be done appropriately, without being influenced by existence of the pad of other neighborhoods.

[0031]Although the pad region for vamps and the pad region for wirebonding, or the pad region for wafer tests is provided to all the terminals in the embodiment of the semiconductor device of this invention, It is also effective for it to be necessary to not necessarily provide to no terminals, and to provide to some terminals.

[0032]While forming the pads 1-20 for vamps in the field 26 where the element on the semiconductor chip 25 exists according to the embodiment by this invention, Wirebonding work can be carried out certainly, without giving a damage to the element on the semiconductor chip 25, since the pad 1A for wirebonding was formed outside the field 26 and these pads of each other were connected.

[0033]Corresponding to each neighborhood of the semiconductor chip 25 which consists of quadrilaterals, two or more pads 1-20 for vamps are formed in the field 26 where the element on the semiconductor chip 25 exists, respectively, While allocating all the pads for vamps of these each neighborhood in center-section slippage of each neighborhood

rather than the pad for vamps of the adjoining neighborhood, Counter said pad for vamps in 20A from two or more pads for wirebonding or pads 1A for wafer tests, respectively, and it allocates along with semiconductor chip each neighborhood, Since these pads of each other belonging to the same input/output terminal were connected, while being able to make the connection structure brief, wirebonding work or wafer test work can be done appropriately, without being influenced by existence of the pad of other neighborhoods.
[0034]Since the shape of the opening 33 of the pad for vamps is circular, the shape of the opening 31 of the pad for wirebonding or the pad for wafer tests is a rectangle and it was made for both aperture shape to differ, Wirebonding work or wafer test work can be done by a technique suitable for each work.
[0035] [Effect of the Invention]While providing the pad for vamps in the field where the element on a semiconductor chip exists according to the 1st invention, Wirebonding work can be carried out certainly, without giving a damage to the element on a semiconductor chip, since the pad for wirebonding was provided outside said field and these pads of each other were connected.
[0036]According to the 2nd invention, it corresponds each neighborhood of the semiconductor chip which consists of quadrilaterals, While providing two or more pads for vamps in the field where the element on a semiconductor chip exists, respectively and allocating all the pads for vamps of these each neighborhood in center-section slippage of each neighborhood rather than the pad for vamps of the adjoining neighborhood, Since these pads of each other that counter said pad for vamps, allocate two or more pads for wirebonding along with semiconductor chip each neighborhood, respectively, and belong to the same input/output terminal were connected, While being able to make the connection structure brief, wirebonding work can be done appropriately, without being influenced by existence of the pad of other neighborhoods.
[0037]According to the 3rd invention, the shape of the opening of the pad for vamps is circular, the shape of the opening of the pad for wirebonding is a rectangle, and since it was made for both aperture shape to differ, wirebonding work can be done by a technique suitable for the work concerned.

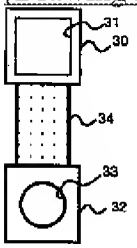
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a top view showing the embodiment of the semiconductor device of this invention.
[Drawing 2]It is an enlarged drawing of the pad region for vamps shown in drawing 1 and the pad region for wirebonding, or the pad region for wafer tests.
[Drawing 3]It is a top view showing the conventional semiconductor chip.
[Drawing 4]It is an enlarged drawing of the pad region for vamps shown in drawing 3.
[Drawing 5]It is the sectional view of a vamp formed on the pad region for vamps shown in drawing 4.
[Description of Notations]
1-20 The pad region for vamps, and 1A-20A The pad region for wirebonding, or the pad region for wafer tests, 25 A semiconductor chip and 26 [The aluminum wiring for vamps, and 33 / The opening of the chip protective film for vamps, aluminum wiring for

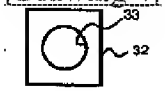
34 pad connection.] The field and 30 in which the element on a chip exists The aluminum wiring for wafer tests, and 31 The opening of the object for wirebonding, or the chip protective film for wafer tests, and 32

DRAWINGS

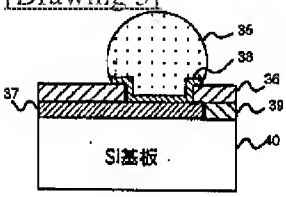
[Drawing 2]



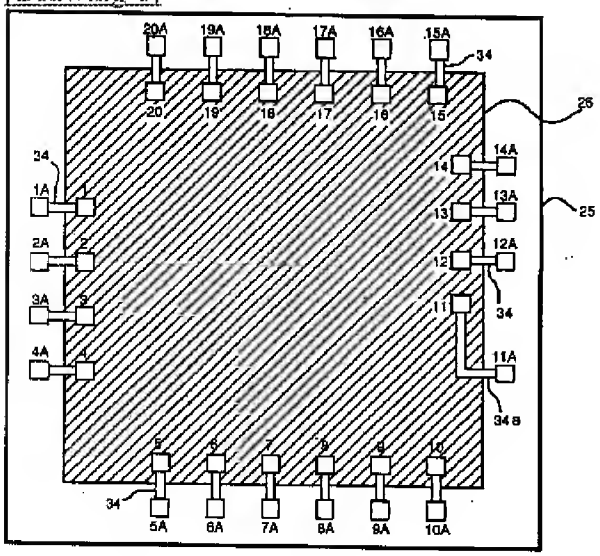
[Drawing 4]



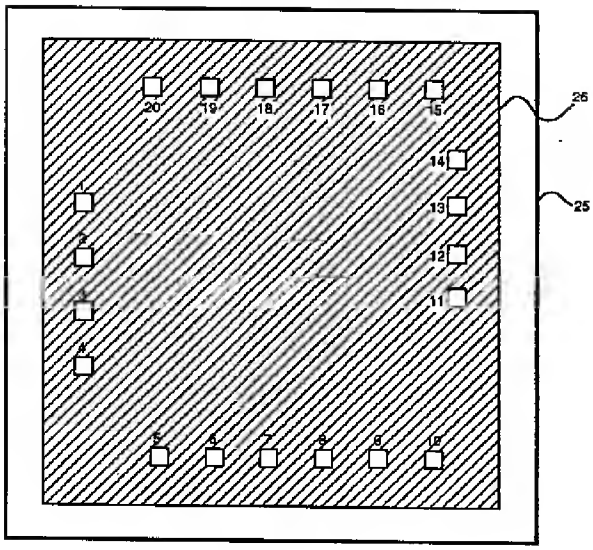
[Drawing 5]



[Drawing 1]



[Drawing 3]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